RAiO

RA8877

Character/Graphic
TFT LCD Controller

Datasheet

Version 1.2

June 5, 2025

RAiO Technology Inc.

1. Introduction

This is the Hardware Functional Specification for the RA8877 TFT LCD Controller. RA8877 supports LVDS type interface (FPD-Link). Including in this document are system block diagrams, Pin information, AC/DC characteristics, each block's function description, detail register descriptions, and power mode control.

1.1 Overview Description

The RA8877 is a low power color LCD Controller with support for up to 512M-bits external SDRAM memory. The RA8877 supports an 8/16-bit asynchronous parallel host bus while providing high performance bandwidth into the external display memory allowing for fast screen updates. The RA8877 also provides support for multiple display buffers, Picture-in-Picture, Opacity control, and display rotation/mirror … etc.

1.2 System Diagram & Chip Diagram

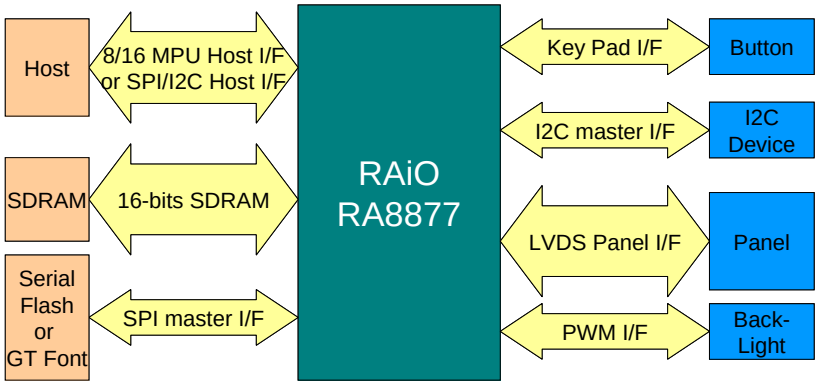


Figure 1-1 : System Diagram

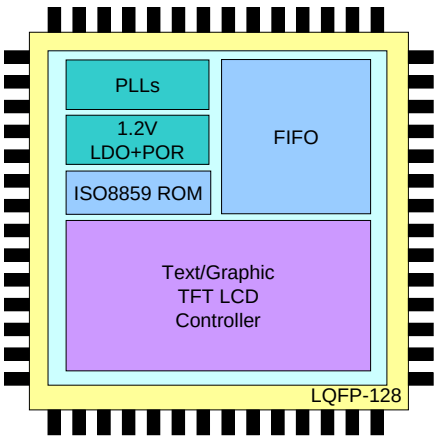


Figure 1-2 : Chip Diagram

2. Features

2.1 Frame Buffer

- Supported SDRAM density:16Mb, 32Mb, 64Mb, 128Mb, 256Mb or 512Mb
- Supported SDRAM configuration: x16
- 16-bit SDRAM bus, maximum frame buffer: 256MB/512MB

2.2 Host Interface

- Support 8080/6800 8/16-bit asynchronous parallel bus interface (MIPI DBI Type A)
  - Provide xnwait event to extend MPU cycle
- Support serial host Interface. Ex. IIC, 3/4-wire SPI
- Mirror and rotation functions are available for image data writes.

2.3 Display Input Data Formats

- 1bpp: monochrome data (1-bit/pixel)
- 8bpp: RGB 3:3:2 (1-byte/pixel)
- 16bpp: RGB 5:6:5 (2-byte/pixel)
- 24bpp: RGB 8:8:8 (3-byte/pixel or 4-byte/pixel)
  - Index 2:6 (64 index colors/pixel with opacity attribute)
  - αRGB 4:4:4:4 (4096 colors/pixel with opacity attribute)

2.4 Display Mode

- Always output 24bpp (RGB 8:8:8) on LVDS channel and support VESA/JEDIA format

2.5 Support Various Panel Resolution

- Embedded LVDS transmitter to support FPD-Link (LVDS interface type panel)
  - LVDS outputs meets or exceed the requirements of ANSI EIA/TIA-644 standard
- Support panel's resolution up-to 2048 dots by 2048 dots. (*Note :The real panel resolution is based on the limitations of pixel clock and color depth.)
  - QVGA: 320 x 240 x 16/18/24-bit LCD panel
  - WQVGA: 480 x 272 x 16/18/24-bit LCD panel
  - VGA: 640 x 480 x 16/18/24-bit LCD panel
  - WVGA: 800 x 480 x 16/18/24-bit LCD panel
  - SVGA: 800 x 600 x 16/18/24-bit LCD panel
  - QHD: 960 x 540 x 16/18/24-bit LCD panel
  - WSVGA: 1024 x 600 x 16/18/24-bit LCD panel
  - XGA: 1024 x 768 x 16/18/24-bit LCD panel
  - WXGA: 1280 x 768 x 16/18/24-bit LCD panel
  - WXGA: 1280 x 800 x 16/18/24-bit LCD panel
  - WXGA: 1366 x 768 x 16/18/24-bit LCD panel

2.6 Display Features

- Provide 4 User-defined 32x32 pixels Graphic Cursor
- Display Window
  The display window is defined by the size of the LCD display. Complete or partial updates to the display window are done through canvas image's setting. The active window size and start position are specified in 8 pixel resolution (horizontal) and 1 line resolution (vertical). Window coordinates are referenced to top left corner of the display window (even when flip is enabled or rotate text, no host side translation is required).

- Virtual display
  Virtual display is available to show an image which is larger than LCD panel size. The image may scroll easily in any direction.
- Picture-in-Picture (PIP) display
  Two PIP windows are supported. Enabled PIP windows are always displayed on top of Main window. The PIP windows sizes and start positions are specified in 4 pixel resolution (horizontal) and 1 line resolution (vertical). Image scrolling can be performed by changing the start address of a PIP window. The PIP1 window is always on top of PIP2 window.
- Multi Buffer
  Multi buffering allows the main display window to be switched among buffers. The number of buffers depends on the external SDRAM size and the desired size of the write buffers. Multi buffering allows a simple animation display to be performed by switching the buffers.
- Wake-up display
  Wake-up display is available to show the display data quickly which data is stored in SDRAM. This feature is used when returning from the Standby mode or Suspend mode.
- Vertical Flip display
  Vertical Flip display functions are available for image data reads. PIP window will be disabled if flip display function enable.
- Color Bar Display
  It could display color bar on panel and need not SDRAM. Default resolution is 640 dots by 480 dots

2.7 Initial Display

- Embed a tiny processor and use to show display data which stored in the serial flash and need not external MPU participate. It will auto execute after power-on, until program execute complete then handover control rights to external MPU. It supports 12 instructions. They are:
  - EXIT: Exit instruction (00h/FFh) -- one byte instruction
  - NOP: NOP instruction (AAh) -- one byte instruction
  - EN4B: Enter 4-Byte mode instruction (B7h) -- one byte instruction
  - EX4B: Exit 4-Byte mode instruction (E9h) -- one byte instruction
  - STSR: Status read instruction (10h) -- two bytes instruction
  - CMDW: Command write instruction (11h) -- two bytes instruction
  - DATR: Data read instruction (12h) -- two bytes instruction
  - DATW: Data write instruction (13h) -- two bytes instruction
  - REPT: Load repeat counter instruction (20h) -- two bytes instruction
  - ATTR: Fetch Attribute instruction (30h) -- two bytes instruction
  - JUMP: Jump instruction (80h) -- five bytes instruction
  - DJNZ: Decrement & Jump instruction (81h) -- five bytes instruction

2.8 Block Transfer Engine (BTE)

- 2D BitBLT Engine
- Copy with ROP & color expansion
- Solid fill & Pattern fill
  - Provide User-defined Patterns with 8x8 pixels or 16x16 pixels
- Opacity (Alpha-Blend) control
  It allows two images to be blended to create a new image which can **then** be displayed using a PIP window. The processing speed of Alpha-blend function varies depending on the image size. Optionally, a single input image can be processed.
  - Chroma-keying function: Mixes images with applying the specified RGB color according to transparency rate
  - Window Alpha-blending function: Mixes two images according to transparency rate in the specified region (fade-in and fade-out functions are available).
  - Dot Alpha-blending function: Mixes images according to transparency rate when the target is a graphics image in the RGB format.

2.9 Geometric Drawing Engine

- Draw dot, Line, Curve, Circle, Ellipse, Triangle, Square & Circular Square

2.10 SPI Master Interface

2.10.1 Text Features

- Embedded 8x16,12x24,16x32 Character Sets of ISO/IEC 8859-1/2/4/5.
- Supporting Genitop Inc. UNICODE/BIG5/GB etc. Serial Character ROM with 16x16/24x24/32X32 dots Font Size. The supporting product numbers are GT21L16T1W, GT30L16U2W, GT30L24T3Y, GT30L24M1Z, and GT30L32S4W, GT20L24F6Y, GT21L24S1W.
- User-defined Characters support half size (8x16/12x24/16x32) & full size
- Programmable Text Cursor for Writing with Character
- Character Enlargement Function X1, X2, X3, X4 for Horizontal/Vertical Direction
- Support Character 90 degree Rotation

2.10.2 DMA function

- Support direct data transfer from external serial flash to frame buffer

2.10.3 General SPI master

- Compatible with Motorola's SPI specifications
- 16 bytes entries deep read FIFO
- 16 bytes entries deep write FIFO
- Interrupt generation after Tx FIFO empty and SPI Tx/Rx engine idle

2.11 IIC Interface

- IIC master interface
  - For the expand I/O device, external touch screen controller for panel control
  - Support Standard mode (100kbps) and Fast mode (400kbps)

2.12 PWM Timer

- Two 16-bit timers
- One 8-bit pre-scalars & One 4-bit divider
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

2.13 Key-scan Interface

- Support up-to 5x5 key matrix (share with the GPIO pin)
- Programmable scan period
- Support long Key & repeat key
- Support up to 2 keys are pressed simultaneously
  Note: Restricted support 3-keys are pressed simultaneously (3-keys cannot form 90°)
- Support Key-Scan Wakeup function

2.14 Power Saving

- Support 3 kind of power saving mode
  - Standby mode, Suspend mode & Sleep mode
- It may wakeup by host, key & external event

2.15 Clock Source

- Embedded programmable PLL for system core clock, LCD panel scan clock and the SDRAM clock
- Single crystal clock input: (XI/XO: 10-15MHz)
- Internal system clock (Maximum 120MHz)
- SDRAM clock (Maximum 166MHz)
- LCD panel scan clock (Maximum 100MHz)

2.16 Reset

- Accept external hardware reset to synchronize with system
- Software command reset

2.17 Power Supply

- I/O voltage: 3.3V +/- 0.3V
- Embedded 1.2V LDO for core power

2.18 Package

- LQFP-128
- Operation temperature: -40℃ ~ 85℃

3. Symbol and Package

3.1 RA8877 Symbol & Pin Assignment

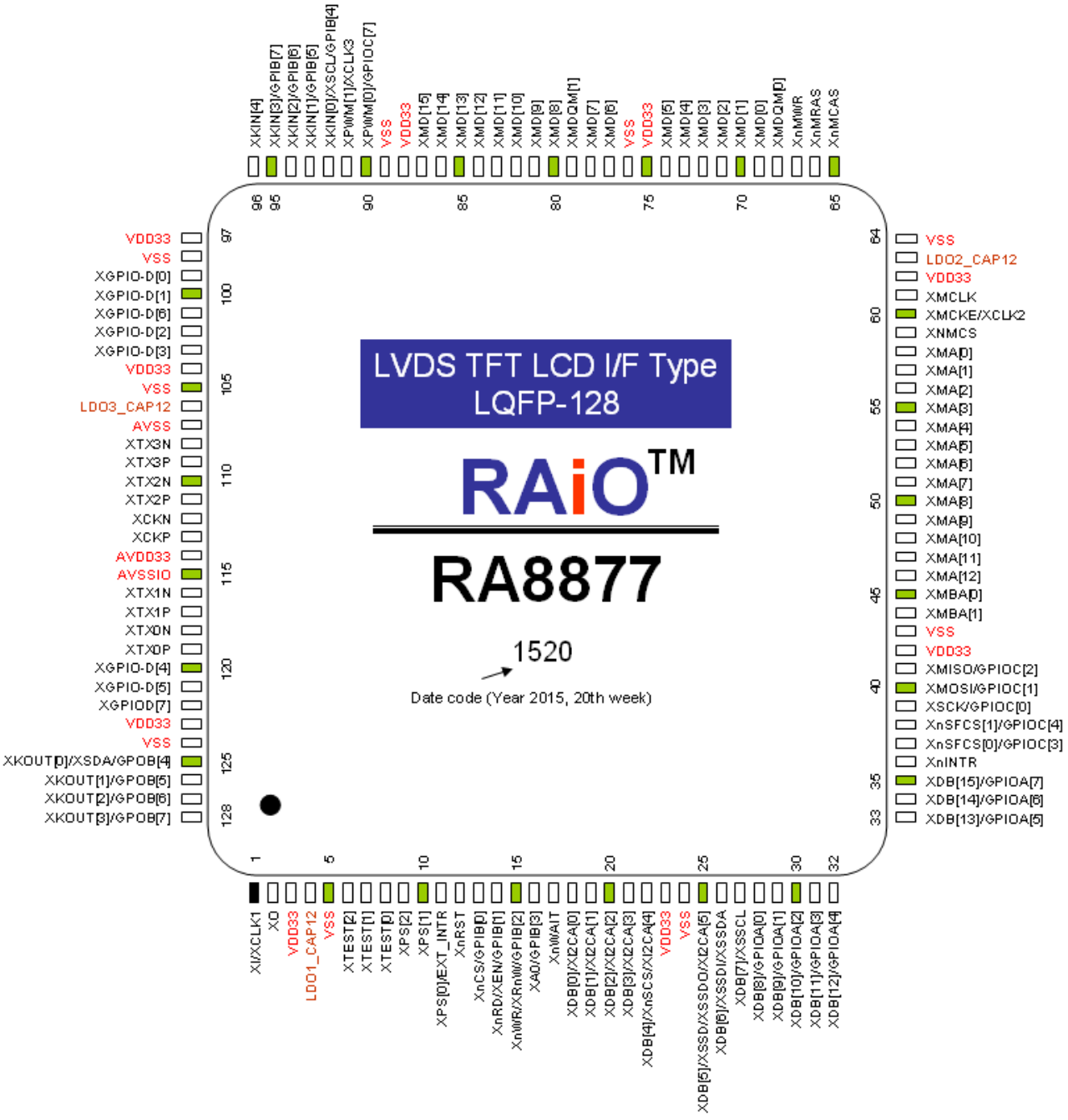
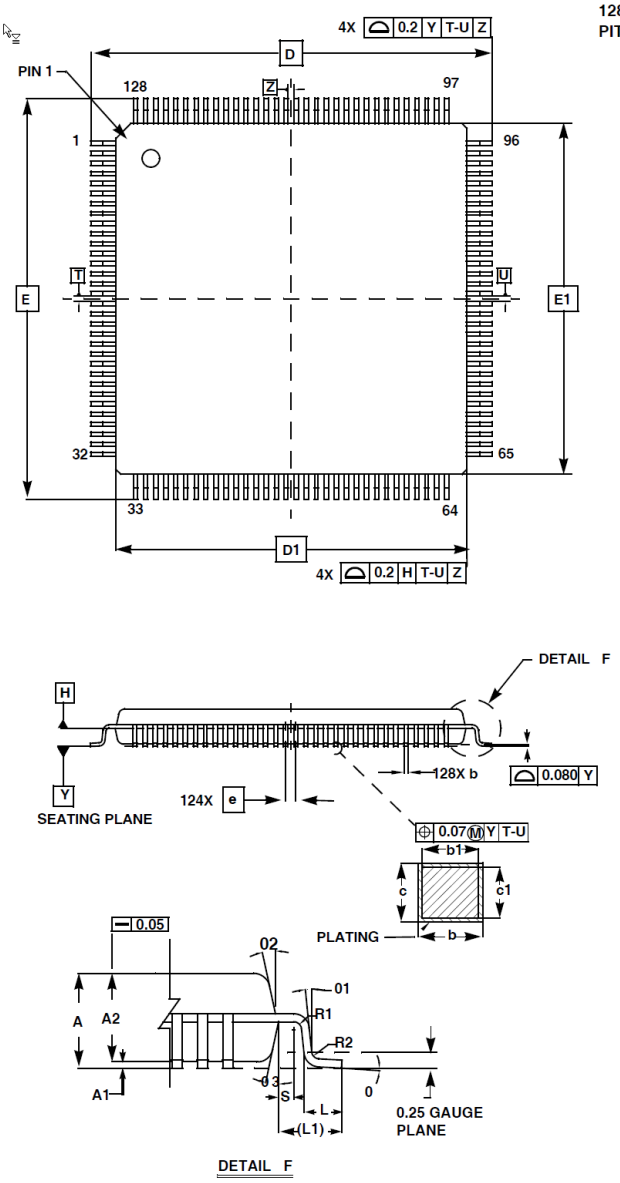


Figure 3-1

3.2 Package Outline Dimensions



Q128.14x14
128 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH

SYMBOL	MILLIMETERS MIN	NOM	MAX	NOTES
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D		16 BSC		-
D1		14 BSC		3
E		16 BSC		-
E1		14 BSC		3
L	0.45	0.60	0.75	-
L1		1.00 REF		-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N		128		-
e		0.40 BSC		-

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NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

Figure 3-2 : RA8877 Package Outline Dimensions

4. Signal Description

4.1 Parallel Host Interface (25 signals)

Pin Name	Dir/Drv.	Pin Description
XDB[15:0]	IO (8mA)	**Data Bus** These are data bus for data transfer between parallel host and RA8877. XDB[15:8] will become GPIO (GPIO-A[7:0]) if parallel host 8080/6800 16-bits data bus mode doesn't set. XDB[7:0] are multiplex with serial host signals if serial host mode set. Please refer to serial host interface section.
XA0	I	**Command / Data Select Input** The pin is used to select command/data cycle. XA0 = 0, status read / command write cycle is selected. XA0 = 1, data read / Write cycle is selected.
XnCS	I	**Chip Select Input** Low active chip select pin. If host I/F set as serial host mode then this pin can be read from GPI-B0. With internal pull-high with resistor.
XnRD (XEN)	I	**Enable/Read Enable** When MPU interface (I/F) is 8080 series, this pin is used as XnRD signal (Data Read), active low. When MPU I/F is 6800 series, this pin is used as XEN signal (Enable), active high. If host I/F set as serial host mode then this pin can be read from GPI-B1. With internal pull-high with resistor.
XnWR (XRnW)	I	**Write/Read-Write** When MPU I/F is 8080 series, this pin is used as XnWR signal (data write) , active low. When MPU I/F is 6800 series, this pin is used as XRnW signal (data read/write control). Active high for read and active low for write. If host I/F set as serial host mode then this pin can be read from GPI-B2. With internal pull-high with resistor.
XnINTR	O (8mA)	**Interrupt Signal Output** The interrupt output for host to indicate the status.
XnWAIT	O (8mA)	**Wait Signal Output** When high, it indicates that the RA8877 is ready to transfer data. When low, then microprocessor is in wait state.
XPS[2:0]	I	**Parallel /Serial Host I/F Select** 00X: (parallel host) 8080 interface with 8/16-bits data bus 01X: (parallel host) 6800 interface with 8/16-bits data bus 100: (serial host) 3-Wire SPI 101: (serial host) 4-Wire SPI 11x: (serial host) IIC ***Note:*** If host I/F set as parallel host mode, then XPS[0] pin is external interrupt pin.

4.2 Serial Host Interface (Multiplex with Parallel Host Interface)

Pin Name	Dir/Drv.	Pin Description
XSSCL (XDB[7])	I	**SPI or IIC Clock** XSSCL, 3-wire, 4-wire Serial or IIC I/F clock.
XSSDI XSSDA (XDB[6])	I	**IIC data /4-wire SPI Data Input** 3-wire SPI I/F: NC, please connect it to GND. 4-wire SPI I/F: XSSDI, Data input for serial I/F. IIC I/F: XSSDA, Bi-direction data for serial I/F
XSSD XSSDO (XDB[5])	IO	**3-wire SPI Data /4-wire SPI Data Output/IIC Slave Address Select** 3-wire SPI I/F: XSSD, Bi-direction data for serial I/F 4-wire SPI I/F: XSSDO, Data output for serial I/F. IIC I/F: XIICA[5], IIC device address bit [5].
XnSCS (XDB[4])	I	**SPI Chip Select/IIC Slave Address Select** XnSCS, Chip select pin for 3-wire or 4-wire serial I/F. IIC I/F : XIICA[4], IIC device address bit [4].
XIICA[3:0] (XDB[3:0])	I	**IIC I/F: IIC Slave Address Select.** XIICA[3:0], 3|4-wire SPI I/F: NC, please connect it to GND. IIC I/F : IIC device address bit [3:0]

4.3 SDR SDRAM Interface (39 signals)

Pin Name	Dir/Drv.	Pin Description
XMCKE (XCLK2)	IO (8mA)	Clock enable **/ Clock 2 input (memory clock)** When XTEST[0] set low, this pin is SDR memory clock enable When XTEST[0] set high, this pin is external clock 2 input for SDR access.
XMCLK	IO (8mA)	SDR memory Clock out It derives from MPLL or XCLK2
XnMCS	O (4mA)	Chip select
XnMRAS	O (4mA)	Command outputs: XnMRAS, XnMCAS and XnMWR (along with XnMCS) define the command being entered
XnMCAS	O (4mA)	Command outputs
XnMWR	O (4mA)	Command outputs
XMBA[1:0]	O (4mA)	Bank address
XMA[12:0]	O (4mA)	Address
XMD[15:0]	I/O (4mA)	Data bus.
XMDQM[1:0]	O (4mA)	Input/Output mask

4.4 Serial Flash or SPI master Interface (5 signals)

Pin Name	Dir/Drv.	Pin Description
XnSFCS0	IO (8mA)	**Chip Select 0 for External Serial Flash/ROM or SPI device** SPI Chip select pin #0 for serial Flash/ROM or SPI device. * If SPI master I/F is disabled then it can be programmed as GPIO (GPIO-C3); default is GPIO-C3 input function.
XnSFCS1	IO (8mA)	**Chip Select 1 for External Serial Flash/ROM or SPI device** SPI Chip select pin #1 for serial Flash/ROM or SPI device. * If SPI master I/F is disabled then it can be programmed as GPIO (GPIO-C4); default is GPIO-C4 input function. *auto pull-high in reset period if xtest[2:1] is not equal to 01b..
XSCK	IO (8mA)	**SPI Serial Clock** Serial clock output for serial Flash/ROM or SPI device. * If SPI master I/F is disabled then it can be programmed as GPIO (GPIO-C0); default is GPIO-C0 input function.
XMOSI (XSIO0)	IO (8mA)	**Master Output Slave Input** Single mode: Data input of serial Flash/ROM or SPI device. For RA8877, it is output. Dual mode: The signal is used as bi-direction data #0(SIO0). Only valid in serial flash DMA mode. * If SPI master I/F is disabled then it can be programmed as GPIO (GPIO-C1); default is GPIO-C1 input function.
XMISO (XSIO1)	IO (8mA)	**Master Input Slave Output** Single mode: Data output of serial Flash/ROM or SPI device. For RA8877, it is input. Dual mode: The signal is used as bi-direction data #1(SIO1). Only valid in serial flash DMA mode. * If SPI master I/F is disabled then it can be programmed as GPIO (GPIO-C2); default is GPIO-C2 input function.

4.5 PWM Interface (2 signals)

Pin Name	Dir/Drv.	Pin Description
XPWM0	IO (8mA)	**PWM signal output 1 / Initial Display Enable** Pull-high this pin will enable Initial Display function. This pin has internal pull-down in reset period to disable Initial Display function by default. i.e. after reset complete, internal pull-down resistor will be disabled. XPWM 0 output mode is decided by configuration register. If PWM function disabled then it can be programmed as GPIO (GPIO-C7), default is GPIO-C7 input function, or output core clock.
XPWM1 (XCLK3)	IO (8mA)	**PWM signal output 2 / Clock 3 input (panel scan clock)** When XTEST[0] set low: XPWM1 set as output mode & output function is decided by configuration register. It may normal XPWM1 function, oscillator clock output or error flag for Scan bandwidth insufficient or Memory access out of range. When XTEST[0] set high: XPWM1 pin is external panel scan clock input

4.6 KEYSCAN Interface (9 signals)

Pin Name	Dir/Drv.	Pin Description
XKIN[0]/ XSCL	IO (8mA)	**Keypad Data Line or GPIs (General Purpose Input)** Keypad data inputs (Default), with internal pull-up resister. XKIN[0] also has IIC master's XSCL function.
XKOUT[0]/ XSDA	O (8mA)	**Keypad Strobe Line or GPOs (General Purpose Output)** Keypad matrix strobe lines outputs with open-drain. (Default). XKOUT[0] also has IIC master's XSDA function.
XKIN[4:1]	I	**Keypad Data Line or GPIs (General Purpose Input)** Keypad data inputs (Default), with internal pull-up resister.
XKOUT[3:1]	O (8mA)	**Keypad Strobe Line or GPOs (General Purpose Output)** Keypad matrix strobe lines outputs with open-drain. (Default).

4.7 LCD Panel LVDS Interface/FPD-Link (12 signals)

Pin Name	Dir/Drv.	Pin Description
AVDD33	P	Analog positive voltage power supply
AVSSIO	P	Analog ground
XTX0P	A	Transmit positive terminal. LVDS signals. Channel 0
XTX0N	A	Transmit negative terminal. LVDS signals. Channel 0
XTX1P	A	Transmit positive terminal. LVDS signals. Channel 1
XTX1N	A	Transmit negative terminal. LVDS signals. Channel 1
XTX2P	A	Transmit positive terminal. LVDS signals. Channel 2
XTX2N	A	Transmit negative terminal. LVDS signals. Channel 2
XTX3P	A	Transmit positive terminal. LVDS signals. Channel 3
XTX3N	A	Transmit negative terminal. LVDS signals. Channel 3
XCKP	A	Output TX clock. Positive terminal. LVDS levels
XCKN	A	Output TX clock. Negative terminal. LVDS levels

4.8 Clock, Reset & Test Mode (6 signals)

Pin Name	Dir/Drv.	Pin Description
XI (XCLK1)	I	**Crystal input/Clock 1 input** The recommended frequency range of the external crystal must be 10MHz. When the XTEST[0] pin is set to low level, the XI (XCLK1) pin is provided to the internal PLL circuit for use. Therefore, in such application conditions, the XI (XCLK1) pin must be connected to an external crystal to generate the relevant clock signals required by RA8877. On the contrary, when the XTEST[0] pin is set to high level, the XI (XCLK1) pin will be used as the input pin of the external clock.
XO	O	**Crystal Output** The XO pin is the output pin of the internal PLL circuit. The XO pin should be connected to an external crystal.
XnRST	I/OC	**Reset Signal input** To avoid noise interfere XnRST signal and cause fake reset behavior, external XnRST level will be admitted only if it keep its signal level at least 256 OSC clocks.
XTEST[0]	I	**Clock Test Mode** Internal pull down. For chip test function, should be connected to GND for normal operation. 0: Normal mode, Use internal PLL clock. 1: bypass internal PLL clock and instead them with CLK1I, CLK2I & CLK3I.
XTEST[2:1]	I	**Chip Test Mode** 00: normal mode 01: Force SPI master I/F pin floating (for in-system-programming) 1X: RESERVED

4.9 Power and Ground

Pin Name	Dir/Drv.	Pin Description
LDO1_CAP12 **LDO2_CAP12** **LDO3_CAP12**	P	**Loading Capacitor for each LDO** Connect a 1uF capacitor to ground.
VDD33	P	**IO VDD** 3.3V IO power input.
VSS	P	**GND** IO Cell/Core ground signal
AVSSIO	P	**Analog IO GND** Analog IO ground signal
AVSS	P	**Analog IO GND** Analog Core ground signal